REMARKS

Status of the Claims

Claims 1-52 were pending.

Claims 1- 52 were rejected.

Please **amend** claims 1, 2, 15, 16, 17, 24, 27, 28, 30, 32, 33, 34, 35, 49, 50, 51, 52 and cancel claims 3, 26.

It is believed that the remarks laid out herein below attend to all rejections and further issues raised in the pending office action dated 30 May 2006.

Drawings

The Examiner objected to the drawings because it was not clear whether the SUM of Figure 8 was deleted or not. The SUM of Figure 8 has been completely deleted. The figures including a Replacement Figure 8 are attached with this response.

Claim Objections

The Examiner listed claim objections to claims 1-31 and provided suggested amendments to the claims. The suggestions are now included in the amended claims. The term "Ethernet transceiver" in claim 1 was amended to "transceiver" rather than amending the dependent claims.

The Examiner objected to claims 16-17 as allegedly being substantially duplicates of claim 15. Claim 15 has been substantially amended, and is essentially, a different claim. Claims 16 and 17 are directed to different subject matter. More specifically, claim 16 limits selection of *off-diagonal* elements of the sub-block processing matrices, and claim 17 limits selection of *diagonal* elements of the sub-block processing matrices.

Claim Rejections

Claim Rejections Under 35USC112

Claims 1-31 are rejected under 35USC112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Amends have been made to claims 1, 2, 24, 32, 33, 34, 35, 49, 50, 51, 52, and the claims are no longer indefinite.

Claims 1, 32, 33, 49-52 were rejected under 35USC101 as being directed to non-statutory subject matter. The listed claims have been amended to either "a receiver receiving a plurality of digital signal streams", or "the transmitter receiving a plurality of digital signal streams for transmission".

Claim Rejections Under 35USC102

The Examiner rejected claims 1, 3-5, 18-37, and 40-52 were rejected as allegedly being anticipated by Jones et al. (US 2004/0212146). Applicants respectfully disagree.

Amended claim 1 includes the following features:

> a receiver receiving a plurality of digital signal streams, at least one of the plurality of digital signal streams being coupled to another of the plurality of digital signal streams;
>
> a domain transformer for transforming sub-blocks of at least one of the plurality of the digital signal streams from an original domain into a lower complexity domain, wherein each sub-block includes less digital signal stream samples than a block, and wherein a block includes enough samples to exceed the joint filter time sample spans of the plurality of digital signal streams;
>
> a processor for joint processing of the transformed sub-blocks of the plurality of digital signal streams, each of the joint processed digital

signal stream sub-blocks being influenced by other digital signal streams sub-blocks; and

an inverse transformer for inverse transforming the joint processed signal streams sub-blocks back to the original domain.

Support for the amendments to claim 1 can be found in the specification and in originally filed claims 1 and 3.

The Examiner stated with regard to old claims 1 and 3, "Jones et al. discloses in Fig. 9 an Ethernet LAN bi-directional transceiver and its method including receiving a plurality of digital streams in sub-blocks provided by Parallel to Serial Converter 408 of Figure 4." The Examiner further states "Jones et al. discloses a sub-block provided by the Parallel to Serial converter 408, which includes less digital signal stream samples than a block.

As far as applicants understand the Examiner's statements, the Examiner appears to be inferring that Jones teaches sub-blocking of block through the use of a parallel to serial converter (indicated in Figure 4 as a parallel to serial converter 408). Applicants believe the Examiner's argument is that the samples of the serial output are a subset of the larger parallel samples of the parallel to serial converter.

Applicants would like to point out that Jones intended the figure element 408 to be a ***serial to parallel converter, not a parallel to serial converter***. That is, the figure element 408 that the Examiner is referring to is **erroneously marked a parallel to serial converter**. The same figure element is also shown in Figure 6 -- 604, Figure 8 – 604, and correctly identified as a serial to parallel converter. In the specification of Jones (paragraph 0068), the *figure element 408 is correctly identified as a serial to parallel converter 408.* Observation of Figure 4 also makes the error of the figure obvious. That is, Figure 4 also includes a parallel to serial converter 438. In order for the circuits to properly operate, the figure element 408 must be a serial to parallel converter.

That said, the output of the serial to parallel converter 408 includes **blocks that include more samples than the input**. Jones does not in any way suggest sub-blocking that includes less digital signal stream samples than a block. The processing is performed on parallel samples of the serial stream, and these sets of samples include more rather than less samples.

Additionally, Jones (and none of the other references) suggest limitations on block or sub-block sample sizes. Amended claim 1 (limitation of old claim 3) specifies that a block includes enough samples to exceed joint filter time sample spans of the plurality of digital signal streams. None of the cited references specify a limitation on block sizes. None of the cited references even suggest sub-blocking. Therefore, there is absolutely not way to construe a limitation on the number of digital samples included within a sub-block (less digital samples than a block).

Amended claim 1 is patentable over the cited prior art.

Claims 2, 4-25, 27-31 are directly or indirectly dependent on claim 1. Therefore, claims 2, 4-25, 27-31 are patentable over the cited prior art. Additionally, these claims rely on sub-blocking which is not taught by the cited references.

Independent claims 32, 33, 34, 35, 49, 50, 51, 52 all include a limitation on the size of blocks, and then further specifies that processing is on sub-blocks that include less samples than the blocks. None of the cited references individually or in combination teach or suggest these features. Therefore, claims 32, 33, 34, 35, 49, 50, 51, 52 are patentable.

Claims 36-49 are directly or indirectly dependent on claim 35. Therefore claims 36-49 are patentable.

Claims 7, 39 include the features that the joint processing comprises sub-block filters, and a subset of the sub-block filters are disabled when the coupling is below a threshold. The Examiner has correctly noted that these features are not taught by the cited prior art.

Claim 10, includes the feature that the diagonal elements of the sub-block processing matrices are adaptively selected. This feature is not taught by the cited prior art. Therefore, claim 10 is additionally patentable over the cited references.

Claim 11 includes the feature that diagonal elements of the sub-block processing matrices are adaptively selected depending upon signal coupling and inter-symbol interference measurements. This feature is not taught by the cited prior art. Therefore, claim 11 is additionally patentable over the cited references.

The Examiner stated that claims 13-17 are patentable over the cited references.

CONCLUSION

For the reasons given above, and after careful review of the cited reference, applicant respectfully submits that Jones and/or Hench do not result in, teach or suggest applicant's claimed invention.

In view of the above Remarks, applicant has addressed all issues raised in the Office Action dated 30 May 2006, and respectfully solicits a Notice of Allowance for claims 1, 2, 4-25, 27-52. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Respectfully submitted,

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